Principal Physical design / Lead Resume

★★★★★ 2.00 /5 (Submit Your Rating)

San Jose, CA

SUMMARY

- Over 20 years experience in ASIC Design / Chip Integration / Circuit Design / RTL design; Over 15 years of managing Physical Design group at STM/Broadcom/Airgo/ Confidential / Confidential Atheros.
- Solid experience in all aspect of IC design including synthesis, low power synthesis, physical aware synthesis, floorplanning, floorplan's phototyping, power planning, clock tree synthesis (CTS), auto placement and routing, timing optimization, power optimization, parasitic extraction, timing closure (STA), signal integrity analysis, static and dynamic IR drop analysis and physical verification.
- Debug Yield on 14LPP with Samsung.
- More than 9 years experience in 28nm/20soc/14LPP/10LPP TSMC/Samsung process, managed taped out more than a dozen working chips in 28nm, SS 14LPP Wlan.
- Strong experience in Synopsys ICC/ICC2/Innovus and Olympus, Talus for RTL - to-GDSII flow (28nm)..
- Familiar with VDSM issues as AOCV, leakage reduction, DFM.
- Experience in low power methodology.
- Familiar with most EDA tools: circuit and logic simulation, implementation, physical verification.
- Managing teams across Geos, cross training and cross execution among team in different working time-zone.

TECHNICAL SKILLS

Synthesis: DC, DCT, DCG.

Place & Route: Synopsys IC compiler, Olympus, EDI, CCopt. UPF/CPF driven flow from front to back.

TA: Prime Time, PTSI, Tweaker, PrimetimeECO.

Circuit simulation: HSPICE.

Logic simulation: Verilog

Physical verification: Calibre.

Extraction: Star RCXT.

Programming: Familiar with TCL.

PROFESSIONAL EXPERIENCE

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Principal Physical design / L

Responsibilities:

- Managed PCIE design, Mixed signal IP design, Managed IP 10nm from 3rd party house.
- Managed Wireless Modem IP Physical Design from Netlist2Gds in 10nm.
- Integrated Analog IP in Mixed signal chip, task included RDL route, PNR, STA and IR drop.
- Use ICC/ICC2/Innovus to implement Place and Route WIFI chip, 802.11ac/802.11ax for PC/Enterprise Router/Mobil product. This is done in 40nm process. This has integrated RF on die, a complete RF/Digital based band, all in one chip. Our group owns DCG-Synthesis to GDS (including STA/IR drop).
- Managed 3 PD parallel projects. Tasks include technical review of concerns and issues, manageing the work around or EDA bug fixes . Working with Corporate CAD to resolve issues as well.
- Experience in managing projects execution across geos, having experience to build remote PD teams from beginning.
- State of the Art Low Power flow with the entire flow is driven from UPF, involve in the trade off in Low Power design to optimize Deep sleep power leakage.
- The physical design include working with package IR drop, working with third party IP, mixed signal block integration, internal IP, 3rd party IP etc ...
- Performance review the whole team, manage the logistic, resolving conflict in a big team env.
- Contribute to the PDCAD flow of 16ff/14LPP/10LPP/7ff, This range from low power flow to advanced process node flow.
- Make sure the ICC tool is keeping up with the DPT of 16ff and 14nm/10nm DRC rule and placement constraint.
- Familiar with whole CPF/UPF flow front to back. UPF driven layout OR CPF driven floorplan.

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Senior PD Manager

Responsibilities:

- We design 4x4 router chip 802.11ac, MIMO-Multiple users.
- We design wifi/bt chip 1x1 which is based on 802.11ac.
- Worked on many timing critical and congestion blocks under tight schedule. Responsibilities were doing UPF synthesis, floor planning, power planning, power routing, placement, routing, parasitic extraction, static timing analysis and physical verification, IR drop (with VCD), STA.
- Used IC Compiler/Talus to implement place and route for multiple ASIC blocks, Redhawk for IR drop.

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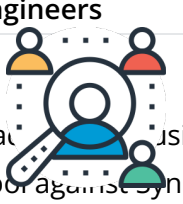
Senior Staff Application engineers



Responsibilities:

- Support Toshiba, Broa[illegible]using Blast fusion tool to build ASIC flow.
- Benchmark Magma tool against Synopsys ICC and SOC Encounter.,
- Own the synthesis/DFT/Blastfusion flow at Magma.
- Successfully brought Blastfusion into LSI who had used ICC previously.
- Started building the group from 2 persons, into 14 PD engineers go work on SOC tapeout:
- HPNA family of chips, HPNA1.0, HPNA2.0 etc, Wifi 802.11a/b/g
- Highly integrated SOC, Wlan/Ethernet/USB, own from netlist to gds, 3 groups taping out 3 chips at the same time. PNR using PC compiler/Astro/Magma. Timing using PTSI